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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,031	03/31/2004	Hiroki Goko	030712-36	3838

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EXAMINER	
MEMULA, SURESH	
ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
10/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,031	GOKO ET AL.	
	Examiner	Art Unit	
	SURESH MEMULA	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2008 and 13 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/31/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is a response to the RCE filed on 08/19/2008. Pursuant to Applicant's amendments and remarks, all previous claim objections and prior art rejections are withdrawn. However, this application is not in condition for allowance in view of the newly considered art detailed below. Claims 1-5 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/13/2008 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-5 are rejected under 35 U.S.C. 102(b)** as being anticipated by US Patent No. 6,536,024 to Hathaway et al. (Hereinafter: Hathaway).

4. As to Claim 1,

a first step for determining a number of clocks different in delay amount (Col. 20, lines 5-7; FIG. 2b: element 212; FIG. 2f, 2g: each modeled stage represents clocks with different delay amount), which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof (Col. 20, lines 8-13; FIG. 2b: element 214), and determining delays in the clocks on the basis of pre-set conditions for constraints of timings (Col. 9, lines 1-5, 22-25, 59-64; FIG. 2b: elements 212-213);

a second step for allocating clocks supplied to respective circuits (FIG. 2b: element 212; FIG. 2f, 2g: each stage represents a clock allocation); and

a third step for optimizing timings on the basis of a list obtained by the timing constraint conditions and the clock allocation (Col. 20, lines 16-19; FIG. 2b: element 216), and determining whether results of analyses of the respective timings correspond to violation of the constraints of timings (FIG. 2b: element 214), wherein the optimization of the timings is repeated according to the constraint violation of the constraints of timings (Col. 20, lines 20-25; FIG. 2b: element feedback loop at output of element 216) and

at least the first and second steps are performed prior to performing a layout design of the semiconductor integrated circuit (Col. 20, lines 5-13; FIG. 2b: element 215; the cited references of Hathaway are performed prior to placement step 215).

5. As to Claim 2, a fourth step for generating the clocks different in the delay amount for the verification of a layout design of the semiconductor integrated circuit (FIG. 2b: elements 214, 217); a fifth step for adjusting skews for each of said clocks (Col. 31, lines 18-24); a sixth step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design (Col. 3, lines 21-26; FIG. 2b: element 217), respectively; seventh step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design (FIG. 2b: elements 215-217) and determining whether analytical results of the respective timings correspond to the constraint violation (FIG. 2b: elements 214-217), wherein the layout adjustment is repeated according to the constraint violation (Col. 20, lines 20-25; FIG. 2b: element feedback loop at output of element 216).

6. As to Claim 3, adjusting the delay of each of the clocks again according to the constraint violation when the constraint violation exists in the third step (Col. 11, lines 8-16; FIG. 2b: elements 214-215).

7. As to Claim 4, a step for adjusting delays set for said clocks according to the constraint violation when the constraint violation occurs in the seventh step (FIG. 2b: element 217).

8. As to Claim 5, wherein adjusting the delays comprises adding an delay at a starting point where data is outputted (Col. 11, lines 8-16; FIG. 2b: element 216-217), and determining the clock delays according to the difference between the added value and the cycle of the clock (Col. 9, lines 1-5, 22-25, 59-64; FIG. 2b: elements 214-217).

Response to Arguments

9. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SURESH MEMULA whose telephone number is (571)272-8046. The examiner can normally be reached on Monday-Friday 8:00-4:30.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Suresh Memula/
Art Unit 2825
October 13, 2008

/Vuthe Siek/
Primary Examiner, Art Unit 2825